IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	William A. Huffman
Serial No.:	09/909,704
Filing Date:	July 20, 2001
Confirmation No.:	9987
Group Art Unit:	2112
Examiner:	Christopher E. Lee
Title:	QUEUE CIRCUIT AND METHOD OF MEMORY ARBITRATION EMPLOYING SAME

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

REPLY BRIEF

In response to the Examiner's Answer dated August 16, 2006, Applicant respectfully submits this reply brief to address matters raised in the Examiner's Answer.

REAL PARTY IN INTEREST

The present Application was assigned to Silicon Graphics, Inc., a Delaware corporation, as indicated by an assignment from the inventor recorded on January 6, 2002 in the Assignment Records of the United States Patent and Trademark Office at Reel 012471, Frames 0824-0826.

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences that will directly affect or be directly affected by or have a bearing on the Board's decision in this pending appeal.

STATUS OF CLAIMS

Claims 1-15 stand rejected pursuant to a Final Action mailed June 24, 2005. Claims 1-15 are all presented for appeal.

STATUS OF AMENDMENTS

A Response to Examiner's Final Action was filed on August 24, 2005 in response to the Final Action mailed June 24, 2005. No additional amendments were made to the claims. The Examiner issued an Advisory Action dated September 13, 2005 which stated that the Response to Examiner's Final Action was considered but that it did not place the application in condition for allowance. A Notice of Appeal and Request for Pre-Appeal Brief Review were on September 26, 2005. A Notice of Panel Decision from Pre-Appeal Brief Review issued on October 14, 2005 indicating that the Application is to proceed to the Board of Patent Appeals and Interferences. Applicant filed an Appeal Brief on November 28, 2005. The Examiner issued an Examiner's Answer on January 17, 2006. Applicant filed a Reply Brief on March 16, 2006. The Examiner issued a Notification of Non-Compliant Appeal Brief on July 13, 2006 in response to an Order Returning Undocketed Appeal to Examiner issued July 5, 2006 by the Board of Patent Appeals and Interferences.

SUMMARY OF CLAIMED SUBJECT MATTER

With respect to Independent Claim 1, a method for managing an arbitration queue 200 having a plurality of entry registers 205 is provided. (See FIGURE 2A, page 11, line 28, to page 12, line 4). Entries 210 received from a processor are introduced into the arbitration queue 200 at the first highest order register 205 (register 63). (See FIGURE 2A, page 12, lines 7-10). The availability of lower order registers 205 are determined. (See page 12, lines 4-7 and lines 28-31). If lower order registers 205 are available, all entries 210 advance one register location in the arbitration queue 200 during each arbitration cycle until it is either serviced or reaches the lowest order register 205 (register 0). (See page 12, lines 11-15). After placement into the arbitration queue 200, each entry 210 is associated with one of a plurality of groups where each group has a different transaction parameter criteria. (See page 16, lines 25-29, and page 18, lines 3-10). A determination is made as to which one of the plurality of groups is selected for servicing. (See page 16, lines 29-31, and page 18, lines 12-14). A particular entry in the selected group is then serviced based on servicing criteria. (See page 18, lines 14-16). After the particular entry is serviced, all higher order entries 210 in the arbitration queue 200 are moved to an adjacent lower order register 205. (See FIGUREs 2B-2C and page 18, lines 19-24).

With respect to Independent Claim 9, a computer system 100 includes a distributed shared memory system 150 and 160, a plurality of processors 140a and 140b generating transactions to the distributed shared memory system 15 and 160, and a memory interface 130. (See FIGURE 1 and page 10, lines 2-13). The memory interface 130 includes a cache memory, an arbitration queue 200, and a memory arbitration processor. (See page 10, lines 14-25; page 11, lines 28-31; and page 13, lines 25-31). The memory interface 130 through the memory arbitration processor performs a memory arbitration scheme by placing transactions as entries in the arbitration queue 200. (See FIGURE 2A and page 12, lines 7-10). After placement in the arbitration queue 200, entries are associated with one of a plurality of groups each having a different transaction parameter criteria. (See page 16, lines 25-29, and page 18, lines 3-10). A particular one of the groups is selected for servicing based on the transaction parameter criteria (See page 16, lines 29-31, and page 18, lines 12-14). A particular entry from the selected one of the groups is then serviced. (See page 18, lines 14-16). The location of the particular entry is marked as idle in the arbitration queue. (See FIGURE 2B and page 12, lines 30-31). The arbitration queue 200 is then collapsed by bringing all higher order entries into adjacent lower order locations to fill the idle location. (See FIGURE 2C and page 12, line 31, to page 13, line 5).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Did the Examiner err in concluding that Claims 1-3 and 5-7 were obvious under 35 U.S.C. §103(a) in view of the combination of U. S. Patent No. 6,160,812 issued to Bauman, et al. in view of U.S. Patent No. 6,185,672 issued to Trull?

2. Did the Examiner err in concluding that Claim 4 was obvious under 35 U.S.C. §103(a) in view of the combination of U. S. Patent No. 6,160,812 issued to Bauman, et al. in view of U.S. Patent No. 6,185,672 issued to Trull and further in view of U.S. Patent No. 6,145,061 issued to Garcia, et al.?

3. Did the Examiner err in concluding that Claim 8 was obvious under 35 U.S.C. §103(a) in view of the combination of U. S. Patent No. 6,160,812 issued to Bauman, et al. in view of U.S. Patent No. 6,185,672 issued to Trull and further in view of In re Yount?

4. Did the Examiner err in concluding that Claims 9-14 were obvious under 35 U.S.C. §103(a) in view of the combination of U.S. Patent No. 5,375,223 issued to Meyers, et al. in view of U. S. Patent No. 6,160,812 issued to Bauman, et al. and further in view of U.S. Patent No. 6,185,672 issued to Trull?

5. Did the Examiner err in concluding that Claim 15 was obvious under 35 U.S.C. §103(a) in view of the combination of U.S. Patent No. 5,375,223 issued to Meyers, et al. in view of U. S. Patent No. 6,160,812 issued to Bauman, et al. and U.S. Patent No. 6,185,672 issued to Trull and further in view of In re Yount?

ARGUMENT

1. Claims 1-3 and 5-7 stand rejected under 35 U.S.C. §103(a) as being obvious over Bauman, et al. in view of Trull. In the Examiner's Answer, there has yet to be an establishment of each of the three criteria for a prima facie case of obviousness.

First, there is no suggestion or motivation in the Bauman, et al. patent or the Trull patent to combine them as proposed by the Examiner. The Examiner has still failed to show that there is some teaching, suggestion, or motivation to combine the Bauman, et al. patent and the Trull patent as proposed. The Bauman, et al. patent is directed to a system for supplying requests to a buffer based on register priority. The Trull patent is directed to an instruction queue for a microprocessor where instructions may be read out of the instruction queue in any order and gaps left by dispatched instructions are filled by shifting the remaining instructions a fixed number of locations within the instruction queue. The Bauman, et al. patent has no queue that remotely operates like the instruction queue of the Trull patent. In fact, the queues of the Bauman, et al. patent operate under a first in first out basis. The only special characteristic of the request buffer of the Bauman, et al. patent is that its four registers may operate together as a FIFO buffer or operate separately as priority registers where the highest priority register will output its contents in a FIFO manner before contents from a lower priority buffer. The Examiner has not cited any language within the Bauman, et al. patent or the Trull patent that would suggest any capability for them to be combined. The only language cited by the Examiner is from the Trull patent and it has no commonality with the operation provided in the Bauman, et al. patent. The rationale provided

by the Examiner for their combination is purely subjective conjecture and speculation with no objective reasoning being provided to support combining the references as has been proposed. The Examiner is merely taking bits and pieces of unrelated subject matter in an improper hindsight attempt at reconstructing the claimed invention. Moreover, the Examiner readily admits on page 15, lines 21-24, of the Examiner's Answer that the claim language was used in supporting the combination of the Bauman, et al. and Trull patents. Since the Examiner has used the claim language in a hindsight attempt to support the combination of the references, the burden to establish the first criteria of a prima facie case of obviousness has not been met.

Moreover, the proposed modification changes the principle of operation of the prior art being modified. The Bauman, et al. patent uses four registers in either a first in first out manner or a first priority manner. The Trull patent uses an instruction queue for out of order dispatch of instructions. Thus, the principle of operation of the Bauman, et al. patent with the Trull patent would be improperly changed by incorporating their respective teachings. The Examiner has yet to explain how the Bauman, et al. patent and the Trull patent can be combined in view of such different functionalities. The Examiner continues to repeat that it would be obvious or clear to one of ordinary skill in the art to combine the references. However, this subjective opinion provided by the Examiner has not been supported by any objective evidence. Therefore, Applicant respectfully submits that the Examiner has failed to establish the first criteria for a prima facie case of obviousness.

With respect to the Examiner's comments in the Examiner's Answer, the Bauman, et al. patent could not handle out of

order instruction dispatch of the Trull instruction queue as it uses the four register buffer as either a FIFO buffer or a priority register buffer with every request in its L0 register always leaving first. The only way a request can leave the four register buffer of the Bauman, et al. patent from a lower priority register in the register priority scheme is if higher priority registers do not contain a request for transport. (See col. 8, lines 33-44, of the Bauman, et al. patent). The Bauman, et al. patent has no queue that operates even remotely like the instruction queue of the Trull patent. The instruction queue of the Trull patent in the system of the Bauman, et al. patent would merely be used as a FIFO queue as the Bauman, et al. patent would not be able to transport requests from any location of the instruction queue and would not need to collapse entries within the instruction queue. The request processing of the Bauman, et al. patent for a multiport switch and the out of order instruction dispatch for a microprocessor of the Trull patent are not in analogous technology fields and would hardly be considered by one of skill in the art let alone in combination as proposed by the Examiner. The Examiner has clearly used two unrelated prior art references to fit the claim language in an improper hindsight attempt to reject the claims of this Application.

Second, a reasonable expectation of success has not been shown by the Examiner. The combination of the Bauman, et al. patent and the Trull patent would not be capable of performing the operation required by the claimed invention. There is no showing by the Examiner that the functions of any of the Bauman, et al. patent and the Trull patent would be able to operate in a single system. There has also been no showing that the combined references would even be able to perform the functionality of the claimed invention. The proposed

combination attempts to combine incompatible processing techniques that have not been shown to be capable of operating according to any degree of predictability. The Bauman, et al. patent would not be able to have the option of either a request buffer with registers combined into a single FIFO unit or separate FIFO priority registers through incorporation of the instruction queue of the Trull patent. The Examiner, without the improper hindsight look through the claimed invention, has not addressed how the proposed combination of the Bauman, et al. patent and the Trull patent would have any success whatsoever let alone a reasonable expectation of success. Therefore, Applicant respectfully submits that the Examiner has failed to establish the second criteria for a prima facie case of obviousness.

With respect to the Examiner's comments in the Examiner's Answer, the Examiner merely states that a reasonable expectation of success is shown by the Trull patent teaching the claimed collapsible queue. By contrast, the Examiner has yet to show any expectation of success that the instruction queue of the Trull patent could be operatively incorporated into the register priority queue system of the Bauman, et al. patent let alone a reasonable expectation of success without resorting to a hindsight comparison to the claimed invention. The Examiner states that Applicant has failed to provide any evidence showing no reasonable expectation of success. However, it is the Examiner's burden to establish this second criteria for a prima facie case of obviousness. Since the Examiner has failed to establish this second criteria, there is no need for Applicant to present any evidence on this issue.

Third, the Examiner has not shown that the proposed Bauman, et al. - Trull combination teaches or suggests all of

the claim limitations. For example, Independent Claim 1 recites ". . . associating each entry after placement in the queue to one of a plurality of groups, each of the plurality of groups having a different transaction parameter criteria; determining which particular one of the plurality of groups to service based on the transaction parameter criteria; servicing a particular entry in the particular one of the plurality of groups based on servicing criteria . . ." By contrast, the Bauman, et al. places packets in its request buffer registers and removes packets therefrom based on either a FIFO buffer or a FIFO register priority scheme. Under the FIFO buffer scheme, every packet in register L0 is serviced first. In the FIFO register priority scheme, packets are grouped by type and then placed into specific request buffer registers that are assigned the corresponding packet type. Thus, under the FIFO register priority scheme, the Bauman, et al. patent groups its transfers prior to placement within its request buffer registers so that its groups can be inserted into corresponding request buffer registers and can be output from the corresponding request buffer registers in a first in first out basis.

Moreover, the Bauman, et al. patent clearly discloses that requests enter request queues in a time ordered manner with the oldest request being at the bottom of the request queue and the youngest request being at the top of request queue. Any grouping of requests in the Bauman, et al. patent is determined prior to placement into a request queue so that the right request can be provided to the right request queue. For example, requests placed into request queue 282 are destined for channel module 112 and thus become grouped prior to placement into request queue 282. Once in request queue 282, there is no further grouping of the requests as

arbitration is performed among all of the requests therein. The claimed invention requires grouping of entries after being placed into a queue and not before as is performed in the Bauman, et al. patent and then servicing of a particular entry of a particular group from the queue. The Examiner has yet to show any grouping of requests being performed in the Bauman, et al. patent after placement into a queue followed by servicing of a particular entry of a particular group from the queue as required in the claimed invention.

The Trull patent performs no grouping whatsoever of instructions within its instruction queue. Thus, even with the use of the queuing operation of the Trull, et al. patent with the request buffer of the Bauman, et al., there would still lack an ability to group entries after placement into a queue and then servicing a particular entry from a particular group from the queue as required by the claimed invention. Therefore, Applicant respectfully submits that Claims 1-3 and 5-7 are patentably distinct from the proposed Bauman, et al. - Trull combination.

With respect to the Examiner's comments in the Examiner's Answer, neither the Trull nor Bauman, et al. patents teach the feature of associating each entry after placement in the queue to one of a plurality of groups. The Examiner readily admits that the Trull patent does not perform any grouping of entries after placement into its instruction queue. The Examiner argues that the Bauman, et al. patent places packets in request queues 252 before being grouped into primary arbitration queue 282 which are copies of channel module request buffers 122. As taught by the Bauman, et al. patent, requests from a port 292 are queued in a single request queue 252. The oldest request in request queue 252 is then sent out to one of four registers in request buffer 122 and copied in

primary arbitration queue 282. Thus, the Bauman, et al. patent fails to disclose any capability to associate a request in a queue 252 to any group after placement therein.

The four registers in channel module request buffer 122 are either set up as a FIFO packet priority queue or a FIFO register priority queue. As a FIFO packet priority queue, a request from request queue 252 is placed into a lowest priority register LM and works its way through registers L2 then L1 before leaving request buffer 122 through highest priority register L0. As a FIFO register priority queue, packets are placed in the registers according to a priority of the packet. Whenever highest priority register L0 contains a packet, it will leave request buffer 122 before any packets from any other register. Packets will leave request buffer 122 from lowest priority register LM only when registers L2, L1, and L0 do not contain any packets. In either the FIFO packet priority queue or FIFO register priority queue implementation of request buffer 122, there is no associating of packets to any groups let alone after placement into the queue structure. As a result, neither the Trull patent nor the Bauman, et al. patent perform the ability to associate each entry after placement in the queue to one of a plurality of groups as required by the claimed invention.

Thus, the Examiner has failed to establish the third criteria for a prima facie case of obviousness. As a result of the improper combination of the references, the lack of any expectation of success for the combination, and the lack of disclosure in the patents being combined by the Examiner, there is an insufficient basis to support the rejection of the claims.

2. Claim 4 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Bauman, et al. in view of Trull and further in view of Garcia, et al. Independent Claim 1, from which Claim 4 depends, has been shown above to be patentably distinct from the proposed Bauman, et al. - Trull combination. Moreover, the Garcia patent does not include any additional disclosure combinable with the Bauman, et al. or Trull patents that would be material to patentability of these claims. Therefore, Applicant respectfully submits that Claim 4 is patentably distinct from the proposed Bauman, et al. - Trull - Garcia, et al. combination.

3. Claim 8 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Bauman, et al. in view of Trull and further in view of In re Yount. Independent Claim 1, from which Claim 8 depends, has been shown above to be patentably distinct from the proposed Bauman, et al. - Trull combination. Therefore, Applicant respectfully submits that Claim 8 is patentably distinct from the proposed Bauman, et al. - Trull - In re Yount combination.

4. Claims 9-14 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Meyers, et al. in view of Bauman, et al. and further in view of Trull. Independent Claim 9 recites ". . . associating entries after placement in the arbitration queue to one of a plurality of groups, each of the plurality of groups having a different transaction parameter criteria; determining which particular one of the plurality of groups to service based on the transaction parameter criteria; servicing a particular entry of the particular one of the plurality of groups . . ." As stated above, the Examiner has not established the three criteria for a prima facie of obviousness. The Examiner has not shown that the Bauman, et al. and Trull patents can be properly combined as proposed let alone for the Meyers, et al. patent to be combined with either the Bauman, et al. or Trull patents according to any objective basis in satisfaction of the first criteria. There has been no mention that the proposed Bauman, et al. - Trull combination provides any expectation of success let alone a reasonable expectation of success, especially with the addition of the Meyers, et al. patent to the proposed combination, to satisfy the second criteria. With respect to the third criteria, the Meyers, et al. patent uses a shift register that receives requests from processors and services the requests according to a processor priority. The Examiner readily admits that the Meyers, et al. patent fails to teach a collapsible arbitration queue as provided in the claimed invention. The Examiner cites the Trull patent to offset this lack of disclosure in the Meyers, et al. patent and support a collapsible queue. However, the Trull patent places instructions into a queue without associating them with a group. To remedy this deficiency, the Examiner cites the Bauman, et al. patent for its grouping technique. However, as

stated above, the Bauman, et al. patent groups its transfers prior to placement within its request buffer under the register priority scheme so that each group can be inserted into a specific register and can be output from the specific register in a first in first out basis. Thus, even with the use of the queuing operation of the Trull, et al. patent with the request buffer of the Bauman, et al. and somehow incorporate the shift register of the Meyers, et al. patent, there would still lack an ability to group entries after placement into a queue followed by servicing of a particular entry of a particular group from the queue as required by the claimed invention. Therefore, Applicant respectfully submits that Claims 9-14 are patentably distinct from the proposed Meyers, et al. - Bauman, et al. - Trull combination.

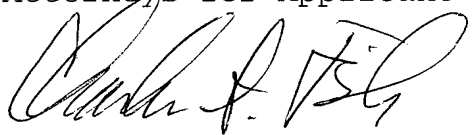
5. Claim 15 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Meyers, et al. in view of Bauman, et al. and Trull and further in view of In re Yount. Independent Claim 9, from which Claim 15 depends, has been shown above to be patentably distinct from the proposed Meyers, et al. - Bauman, et al. - Trull combination. Therefore, Applicant respectfully submits that Claim 15 is patentably distinct from the proposed Meyers, et al. - Bauman , et al. - Trull - In re Yount combination.

CONCLUSION

Applicant has clearly demonstrated that the present invention as claimed is clearly distinguishable over all the art cited of record, either alone or in combination, and satisfies all requirements under 35 U.S.C. §§101, 102, and 103, and 112. Therefore, Applicant respectfully requests the Board of Patent Appeals and Interferences to reverse the final rejection of the Examiner and instruct the Examiner to issue a Notice of Allowance of all claims.

The Commissioner is hereby authorized to charge any fees or credit any overpayments to Deposit Account No. 02-0384 of BAKER BOTTS L.L.P.

Respectfully submitted,
BAKER BOTTS L.L.P.
Attorneys for Applicant



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APPENDIX A

1. (Previously Presented) A method of managing an arbitration queue having a plurality of queue entries comprising:

introducing entries into the queue at a first, highest order queue location;

determining if lower order queue locations are available;

if lower order queue locations are available, moving all higher order queue location contents to an adjacent lower order queue location per cycle until all lower order locations are filled;

associating each entry after placement in the queue to one of a plurality of groups, each of the plurality of groups having a different transaction parameter criteria;

determining which particular one of the plurality of groups to service based on the transaction parameter criteria;

servicing a particular entry in the particular one of the plurality of groups based on servicing criteria; and

moving all higher order queue entries, with respect to the particular entry being serviced, to an adjacent lower order location in the queue.

2. (Original) The method of claim 1, further comprising the step of marking a location of a serviced entry as idle.

3. (Original) The method of claim 2 wherein the moving step further comprises:

for higher order locations with respect to the idle location, writing the contents of higher order queue locations into adjacent lower order queue locations; and

for lower order locations with respect to the idle location, rewriting the current entry into the location.

4. (Original) The method of claim 1, further comprising the step of initializing all queue locations to an idle state prior to the step of introducing entries into the queue.

5. (Previously Presented) The method of Claim 1, wherein moving all higher order queue entries further comprises:

providing a plurality of registers corresponding to a number of entries in the queue, the plurality of registers being arranged in a linear array from a highest order register to a lowest order register;

for each register, selectively providing to each register an entry from that register or an entry from a higher order register.

6. (Previously Presented) The arbitration queue circuit according to claim 5, wherein entries are added to the queue via the highest order register.

7. (Original) The arbitration queue circuit according to claim 6, wherein the plurality of registers each have an entry output such that an entry can be removed from any location in the queue.

8. (Original) The arbitration queue circuit according to claim 7, wherein the plurality of registers includes 64 registers.

9. (Previously Presented) A computer system comprising:

a distributed shared memory system;

a plurality of processors generating transactions to said distributed shared memory system; and

a memory interface interposed between said distributed shared memory system and said plurality of processors, said memory interface having cache memory, a collapsible arbitration queue having a plurality of entry locations, and a memory arbitration processor for servicing transactions from said plurality of processors, the memory arbitration processor performing a memory arbitration scheme comprising:

placing transactions as entries in the arbitration queue;

associating entries after placement in the arbitration queue to one of a plurality of groups, each of the plurality of groups having a different transaction parameter criteria;

determining which particular one of the plurality of groups to service based on the transaction parameter criteria;

servicing a particular entry of the particular one of the plurality of groups;

marking a location of the particular entry in the arbitration queue as idle; and

collapsing the arbitration queue by bringing all higher order entries into adjacent lower order locations in the queue to fill the idle location.

10. (Original) The computer system according to claim 9, wherein the collapsing operation comprises:

for higher order queue locations with respect to the idle location, writing the contents of higher order queue locations into adjacent lower order queue locations; and

for lower order queue locations with respect to the idle location, rewriting the current entry into the location.

11. (Original) The computer system according to claim 9, wherein the plurality of entry locations includes a highest order location and a lowest order location, and wherein entries are added to the queue via the highest order location.

12. (Original) The computer system of claim 9, wherein the arbitration queue comprises:

a plurality of registers corresponding to the number of entries in the queue;

a plurality of 2:1 multiplexers interposed between said registers such that one multiplexer is interposed between a higher order register and a subsequent register, the output of said higher order register being coupled to a first input of said one multiplexer, the output of said subsequent register being coupled to a second input of said one multiplexer, an output of said one multiplexer being coupled to said subsequent register, and a mux control line being coupled to said one multiplexer to direct the contents of one of said first and second multiplexer inputs to the multiplexer output; whereby the mux control line associated with the higher order register and subsequent register determines whether the subsequent register is refreshed with its current contents or receives the contents of the higher order register.

13. (Original) The arbitration queue circuit according to claim 12, wherein the plurality of registers includes a highest order register and a lowest order register, and wherein entries are added to the queue via the highest order register.

14. (Original) The arbitration queue circuit according to claim 13, wherein the plurality of registers each have an entry output such that an entry can be removed from any entry in the queue.

15. (Original) The arbitration queue circuit according to claim 14, wherein the plurality of registers includes 64 registers.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None

CERTIFICATE OF SERVICE

None